CLAIMS

Please amend the claims as shown in the following claim listing.

1. (Currently amended) A logic circuit comprising:

data flow logic; and

control flow logic to select and fetch a trace descriptor for processing, the fetched trace descriptor including at least one dependency descriptor, the control flow logic to dispatch to the data flow logic a dependency descriptor including dependency information for an instruction sequence and an address of the instruction sequence; ~~and~~

the data flow logic coupled to the control flow logic to receive the dispatched dependency descriptor, to fetch the instruction sequence using the address from the received dependency descriptor, and to execute the instruction sequence according to the dependency information in the received dependency descriptor.

2. (Currently amended) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic and the data flow logic, the storage area to store the dependency descriptor ~~from the fetched trace descriptor~~dispatched by the control flow logic.

3. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic, the storage area to store trace descriptors.

4. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the data flow logic, the storage area to store instructions contiguously based on dependency information.

5. (Previously presented) The logic circuit of claim 1 comprising a storage area coupled to the data flow logic and control flow logic, the storage area to store live-out data.

6. (Currently amended) The logic circuit of claim 1 comprising a storage area coupled to the control flow logic, the storage area to map ~~live-in and live-out data~~dependency information.

7. (Canceled).

8. (Currently amended) The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-in ~~data~~information for a plurality of dependency descriptors in the trace descriptor.

9. (Currently amended) The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-out ~~data~~information for a plurality of dependency descriptors in the trace descriptor.

10. (Currently amended) A computer system comprising:

at least one memory device to store trace descriptors and instruction sequences;

a bus coupled to the at least one memory device;

control flow logic to select and fetch one of the trace descriptors, the fetched trace descriptor including a plurality of dependency descriptors having locations of corresponding instruction sequences and having dependency information for corresponding instruction sequences; and

data flow logic coupled to the control flow logic to receive a dependency descriptor dispatched from the control flow logic, to fetch an instruction sequence corresponding to the received dependency descriptor, and to execute the fetched instruction sequence according to dependency information in the received dependency descriptor.

11. (Previously presented) The computer system of claim 10 comprising an issue window coupled between the control flow logic and the data flow logic, the issue window to store the dependency descriptor dispatched from the control flow logic.

12. (Canceled).

13. (Currently amended) The computer system of claim 10 wherein the at least one memory ~~unit~~device is to store an instruction sequence contiguously based on dependency information.

14. (Previously presented) The computer system of claim 10 comprising a storage area coupled to the data flow logic and control flow logic, the storage area to store live-out data.

15. (Currently amended) The computer system of claim 10 comprising a storage area coupled to the control flow logic, the storage area to map ~~live-in and live-out data~~dependency information.

16. (Canceled).

17. (Currently amended) The computer system of claim 10 wherein the fetched trace descriptor includes aggregate live-in ~~data~~information for dependency descriptors in the fetched trace descriptor.

18. (Currently amended) The computer system of claim 10 wherein the fetched trace descriptor includes aggregate live-out ~~data~~information for dependency descriptors in the fetched trace descriptor.

19. (Currently amended) The computer system of claim 10 wherein dependency information ~~of~~in the received dependency descriptor includes live-in and live-out ~~data~~information.

20. (Currently amended) A method of processing instructions comprising:
selecting and fetching a trace descriptor in accordance with program control flow;

identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions and an address of the set of instructions;

dispatching the dependency descriptor for execution;

fetching the set of instructions using the address ~~in~~from the dispatched dependency descriptor; and

executing the set of instructions according to ~~the~~ dependency information in the dispatched dependency descriptor.

21. (Previously presented) A method according to claim 20 comprising:

updating live-out data in a storage area.

22. (Currently amended) A method according to claim 20 comprising:

storing the ~~identified~~ dependency descriptor from control flow logic into a storage area; and

reading the dependency descriptor out of the storage area into data flow logic.

23. (Previously presented) A method according to claim 20 wherein the fetching of the set of instructions is completed just in time for execution.

24. (Previously presented) A method according to claim 20 wherein the executing comprises executing instructions out of order.

25. (Currently amended) A method according to claim 21 comprising:

updating ~~the~~an architectural state using data in the storage area.

26. (Previously presented) A method according to claim 25 comprising:

recovering an earlier architectural state after a misprediction using data in the storage area.

27. (Previously presented) A method according to claim 20 wherein the selecting comprises predicting a next trace descriptor to process.

28. (Currently amended) A machine-readable medium that provides instructions, which when executed by a machine cause the machine to perform operations comprising:

selecting and fetching a trace descriptor in accordance with program control flow;

identifying from the fetched trace descriptor a dependency descriptor including dependency information for a set of instructions and an address of the set of instructions;

dispatching the dependency descriptor for execution;

fetching the set of instructions using the address ~~in~~from the dispatched dependency descriptor; and

executing the set of instructions according to ~~the~~ dependency information in the dispatched dependency descriptor.

29. (Previously presented) The machine-readable medium of claim 28, wherein the operations comprise:

updating live-out data in a storage area.

30. (Previously presented) The machine-readable medium of claim 28, wherein the operations comprise:

storing the dependency descriptor in an issue window by control flow logic; and

reading the dependency descriptor out of the issue window into data flow logic.

31. (Previously presented) The logic circuit of claim 1 wherein the fetched trace descriptor includes a plurality of dependency descriptors having addresses of corresponding instruction sequences and having dependency information for corresponding instruction sequences.

32. (Currently amended) The logic circuit of claim 1 wherein the dependency information includes live-in ~~data~~information.

33. (Currently amended) The logic circuit of claim 1 wherein the dependency information includes live-out ~~data~~information.